Form PTO-1449 U.S. DEPARTMENT OF COMMERCE ATTY. DOCKET NO. MI22-1896 SERIAL NO. PATENT AND TRADEMARK OFFICE 09/633,556 LIST OF ART CITED BY APPLICANT APPLICANT (Use several sheets if necessary) Gurtej S. Sandhu et al. FILING DATE GROUP August 7, 2000 U.S. PATENT DOCUMENTS Date *Examiner Document Name Class Subclass Filing Date Number Initial If Appropriate 5,032,545 07/91 Doan et al. ΑB 07/95 5,436,481 Egawa et al. AC 5,378,645 01/95 Inoue et al. 5,258,333 11/93 Shappir et al. 5,518,946 05/96 Kuroda 5,445,999 08/95 Thakur et al. ÁG 5,382,533 01/95 Ahmad et al. 5,663,077 09/97 Adachi et al. 5,026,574 06/91 Economu et al. 5,026,574 06/91 Economu et al. 5,612,558 Harshfield 5,719,083 Komatsu FOREIGN PATENT DOCUMENTS Date Document Class Subclass Country Translation Number Yes No AΜ PCT AN AO ΑP AQ OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.) Wolf, S., "Silicon Processing for the VLSI Era", Lattice Press 1990, Vol. 2, pp. 212-213. Wolf, S., "Silicon Processing for the VLSI Era", Lattice Press 1990, Vol. 2, pp. 188-189, 194-195, 609-614. The Effect of Nitrogen Incorporation into the Gate Oxide By Using Shallow Implantation of Nitrogen and Drive-In Proecess", IEEE 1996, pp. 32-35. EXAMINER DATE CONSIDERED *EXAMINER: Initial if reference considered, whether of not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

S:\M122\1896\ID2.wpd

A2720115921N

Form PTO-1449 ATTY. DOCKET NO. MI22-1896 U.S. DEPARTMENT OF COMMERCE SERIAL NO. PATENT AND TRADEMARK OFFICE 09/633,556 LIST OF ART CITED BY APPLICANT APPLICANT (Use several sheets if necessary) Gurtej S. Sandhu et al. FILING DATE GROUP August 7, 2000 2813 U.S. PATENT DOCUMENTS Class Date Subclass Document Name *Examiner Filing Date Number Initial If Appropriate 5,760,475 06/98 Cronin AA ΑB 5,834,372 11/98 Lee 04/96 AC 5,619,057 Komatsu AD 5,633,036 05/97 Seebauer et al. ΑE 6,054,396 04/00 Doan 6,174,821 01/01 Doan 5,939,750 08/99 Early ΑH 5,254,489 10/93 Nakata 5,464,792 11/95 Tseng et al. 5,620,908 04/97 Inoh et al. ΑK 5,716,864 02/98 Abe 5,972,783 10/99 Arai et al. FOREIGN PATENT DOCUMENTS Date Class Subclass Country Translation Document Number Yes No AM AN ΑO ΑP AQ OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.) AR Doyle, B. et al., "Simultaneous Growth of Different Thickness Gate Oxides in Silicon CMOS Processing", IEEE Vol. 16 (7), July 1995, Kuroi, T. et al., The Effects of Nitrogen Implantation Into P+Poly-Silicon Gate on Gate Oxide Properties', 1994 Sympos. on VLS1 Technology Digest of Technical Papers, IEEE 1994, pp. 107-108. ΑS Liu, C.T. et al., "Multiple Gate Oxide Thickness for 2GHz System-on-a-Chip Technologies", IEEE 1998, pp. 589-592. AT EXAMINER DATE CONSIDERED *EXAMINER: Initial if reference considered, whether citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communicati n to applicant.

